REMARKS

Claims 1–14 are pending in the application.

Claims 1–14 have been rejected.

No claims have been allowed.

Reconsideration of the claims is respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 102

Claims 1, 4 and 8 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,859,846 to *Kim et al.* The rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Independent claims 1 and 4 each recite a controller and/or switching element receiving time division multiplex (TDM) data on an originating port and mapping that received TDM into a predetermined (ATM) packet slot permanently assigned to the origination port. In the present invention, time division multiplexing transmission through an ATM switch is achieved by assigning each of a plurality of access ports/controllers a predetermined slot within each ATM cell, then

switching data, if any, available from the corresponding access port/controller into the assigned slot within every ATM cell. Such a feature is not shown or suggested by the cited reference. *Kim et al* discloses a packet-based data transmission system comprising a synchronous digital hierarchy (SDH), essentially a synchronous output interface for an ATM switch. The switch module controller 70 simply controls buffering of received ATM cells for synchronous transmission based on routing (VPI/VCI) information therein:

> In each line interface circuit 10, the input port driver 11 converts an input optical signal into an electrical signal and recovers a clock signal from the converted electrical signal. The input port driver 11 also extracts an SDH transmission frame from the converted electrical signal in response to the recovered clock signal. The extracted SDH transmission frame contains cell data with a fixed length and a connection identifier VPI/VCI. Then, the input port driver 11 appends cell destination information (routing tag) to the extracted SDH transmission frame and outputs the resultant SDH transmission frame and the recovered clock signal to all the switch output multiplexers 20 through the input dedicated bus B2. Further, the input port driver 11 extracts a signalling cell or a network managing cell terminating at the system from the converted electrical signal and outputs the extracted signalling cell or network managing cell to the switch call processing controller 60 through the internal dedicated bus B6.
>
> Each switch output multiplexer 20 is adapted to receive successive cells from the input port drivers 11 in the line interface circuits 10 through the input dedicated buses B2. Each of the received cells contains cell data, a cell enable signal CEN, a start-of-cell signal SOC and a synchronous clock signal CLK. The switch output multiplexer 20 performs a received cell selection operation using input port dedicated temporary storage means (internal buffers). In other words, the switch output multiplexer 20 temporarily stores the received cells in the temporary storage means and preferentially reads the cells stored in ones of the temporary storage means corresponding to ones of the input port drivers 11 with high generation frequency. Then, the switch output multiplexer 20 stores the read cells in an output buffer and outputs the stored cells in the form of a cell stream synchronously with an external network synchronous clock signal.

> The switch module controller 70 is adapted to output a control signal to each switch output multiplexer 20 through a control dedicated bus B9 to control it. The switch module controller 70 checks operation and malfunction states of each switch output multiplexer 20 and reports the checked result to the switch maintenance controller 50 which is a managing processor. Further, the switch module controller 70 performs a duplexed function of replacing (board-replacing) a faulty one of the switch output multiplexers 20 with a normal one of the switch output multiplexers 20.
>
> The output port driver 12 in each line interface circuit 10 receives a cell stream from the corresponding switch output multiplexer 20 through the output dedicated bus B3. Then, the output port driver 12 removes the routing tag from the received cell stream, translates a channel identifier in the connection identifier VPI/VCI and transfers the resultant SDH transmission frame to an adjacent node. Also, the output port driver 12 receives the signalling cell or the network managing cell from the switch call processing controller 60 through the internal dedicated bus B7 and transfers the received signalling cell or network managing cell to the adjacent node within the limits of no effect on a user service.

Kim et al, column 5, line 63 through column 6, line 22. The switch module controller 70 of *Kim et al* does not receive non-packetized TDM data as recited in the claims, or map data into predetermined packet slots based on an originating port on which the data was received, as recited in the claims. Any mapping within the system disclosed in *Kim et al* is not into preassigned packet slots, but instead involves complete cells mapped onto predefined paths or circuits identified by the virtual path/circuit routing information within the cell.

Independent claim 8 recites receiving packet data from a plurality of access controllers and separately switching data from each of the access controller into a corresponding preassigned packet slot for the destination. In the present invention, TDM data initially switched into a packet slot preassigned to an origination port is, upon receipt of the packet at a node controller, switched into a different packet slot preassigned to destination port. Such a feature is not shown or suggested by

the cited reference. *Kim et al* switches complete cells based on virtual path/circuit identifiers within received packets or cells, not packet slots based on slot assignments for each destination port.

Accordingly, the Applicants respectfully request the Examiner withdraw the § 102(e) rejection of Claims 1, 4 and 8.

II. REJECTION UNDER 35 U.S.C. § 103

Claims 2–3, 5–7, 9 and 13–14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Kim et al* in view of U.S. Patent No. 6,088,359 to *Wicklund et al.* The rejection is respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

As noted above, independent claims 1, 4 and 8 each recite features not shown or suggested by *Kim et al.* Such features are also not shown or suggested by *Wicklund et al. Wicklund et al* discloses processing all cell rate information resource management packets at a single available bit rate (ABR) server coupled to an ATM switch. *Wicklund et al* does not address TDM data, mapping such data into preassigned packet slots based on origination port, or mapping slots within a received packet into other packet slots based on destination port. At most, *Wicklund et al* discloses only switching of complete cells, and then only on an as-available basis rather than slot assignments for origination and destination ports.

Claim 2 recites that the destination port associated with each incoming packet slot is transmitted on a separate message between the controller, the switching element and a call server.

In the present invention, a call server determines originating and destination communication lines for calls and sends messages to the node controller to switch data from the origination line to the destination line, by switching the data into a preassigned packet slot for the origination line and then into a preassigned packet slot for the destination line. Such a feature is not shown or suggested by the cited references. As conceded in the Office Action, *Kim et al* does not teach or suggest a separate server. *Wicklund et al* discloses an available bit rate server 55 to which resource management cells are directed, with the server performing necessary calculations for explicit rate ABR transmission within an ATM switch. ABR server does not provide information relating to origination and destination lines of a call, but instead merely provides centralized data accumulation and processing for cell rate information, allowing the rate of cell transmission to be dynamically adapted to variable bandwidth conditions. The ABR server 55 in *Wicklund et al* does not comprise a call server, as that term is employed ordinarily within the relevant art or within the specification. Moreover, neither reference provides a basis for reasonable expectation of success in incorporating the ABR server of *Wicklund et al* into the system disclosed in *Kim et al*, nor any basis for concluding that such incorporation would achieve the claimed invention.

Claim 3 specifies that the call server instructs the switching elements on switching packet slot data into packet slots assigned to the port for the destination line. Such a feature is not shown or suggested by either of the cited reference, taken alone or in combination. Neither *Kim et al* nor *Wicklund et al* teaches or suggests a separate server instructing switching elements on routing of data in general, or packet slots in particular.

Claim 5 recites a call server employed to determine a destination port. Such a feature is not shown or suggested by either of the cited reference, taken alone or in combination. As conceded in the Office Action, *Kim et al* does not teach or suggest a separate server. As noted above, the ABR server 55 in *Wicklund et al* is not a call server, and in particular may not be employed to determine destination ports since that server merely computes and updates cell rate information from and within resource management cells routed therethrough.

Claim 6 recites a look-up table within the call server to identify the packet slot corresponding to a destination port. Such a feature is not shown or suggested by either of the cited reference, taken alone or in combination. A look-up table of the type recited is not, as asserted in the Office Action, inherent to the ABR server 55, which does not maintain data relating to call switching and in particular does not address packet slots. Therefore ABR server 55 has no inherent need for a look-up table relating to packet slots, or a look-up table associating packet slots with destination ports.

Claim 7 recites that the call server includes an input/output controller sending a message to a switching element instructing the switching element to switch TDM data within a received packet out of the slot assigned to the origination port and into the slot assigned to the destination port. Such a feature is not shown or suggested by either of the cited reference, taken alone or in combination. *Wicklund et al* does not teach or suggest that ABR server 55 instructs a switching element on switching data from one packet slot to another in general, or switching from slot to slot based on origination and destination ports in particular.

Independent claim 9 recites receiving incoming ATM cells, receiving switching directions for individually switching segments of the incoming cells into slot within outgoing cells, and performing the switching specified in the received switching directions on the data within the received ATM cells. Such a feature is not shown or suggested by either of the cited reference, taken alone or in combination. *Kim et al* does not teach or suggest that switch output multiplexers 20 switch packet segments (octets or slots) for certain locations in incoming cells to different locations within outgoing cells, but instead teaches only that switch output multiplexers 20 switch complete cells from input port drivers 11 to output port drivers 12. *Wicklund et al* does not teach or suggest that switch core 54 switches data based on instructions received from an external source, or that packet slots are switched from one location within an incoming cell to another location within an outgoing cell. Pursuant to MPEP § 2144.03, Applicants respectfully traverse the assertion that octet switching as recited in the claims (i.e., to reorder packet slots from a sequence based on origination ports to a sequence based on destination ports) is well-known.

Claim 12 recites a buffer and a time switch controller sequentially writing slots within incoming cells into buffer entries, then reading the buffer entries using a sequence of read addresses supplied based on the externally generated switching directions. Such a feature is not shown or suggested by either of the cited reference, taken alone or in combination. Neither *Kim et al* nor *Wicklund et al* teach or suggest a mechanism for reordering packet octets or slots between incoming and outgoingin general

Independent claim 13 recites receiving packets from a plurality of controllers containing data from various originating ports each in a particular packet slot assigned to the origination port, receiving a message from a call server, and switching data from the packet slot assigned to the originating port into a packet slot assigned to the destination port in response to the received message. Such a feature is not shown or suggested by either of the cited reference, taken alone or in combination. Neither *Kim et al* nor *Wicklund et al* teach or suggest switching packet slot data from an incoming packet slot assigned to the originating port to an outgoing packet slot assigned to the destination port under control of a message from a call server.

Claim 14 recites that the mapping of incoming packet slots to outgoing packet slots is employed until another message is received from the call server. Such a feature is not shown or suggested by either of the cited reference, taken alone or in combination. Neither *Kim et al* nor *Wicklund et al* teach or suggest a persistent packet slot mapping configuration maintained until dynamically replaced by a new mapping configuration.

Accordingly, the Applicants respectfully request withdrawal of the § 103 rejection of Claims 2–3, 5–7, 9 and 13–14.

III. CONCLUSION

As a result of the foregoing, the Applicants assert that the remaining Claims in the Application are in condition for allowance, and respectfully request an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: 11-14-02

Daniel E. Venglarik
Registration No. 39,409

P.O. Drawer 800889
Dallas, Texas 75380
(972) 628-3621 (direct dial)
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *dvenglarik@davismunck.com*